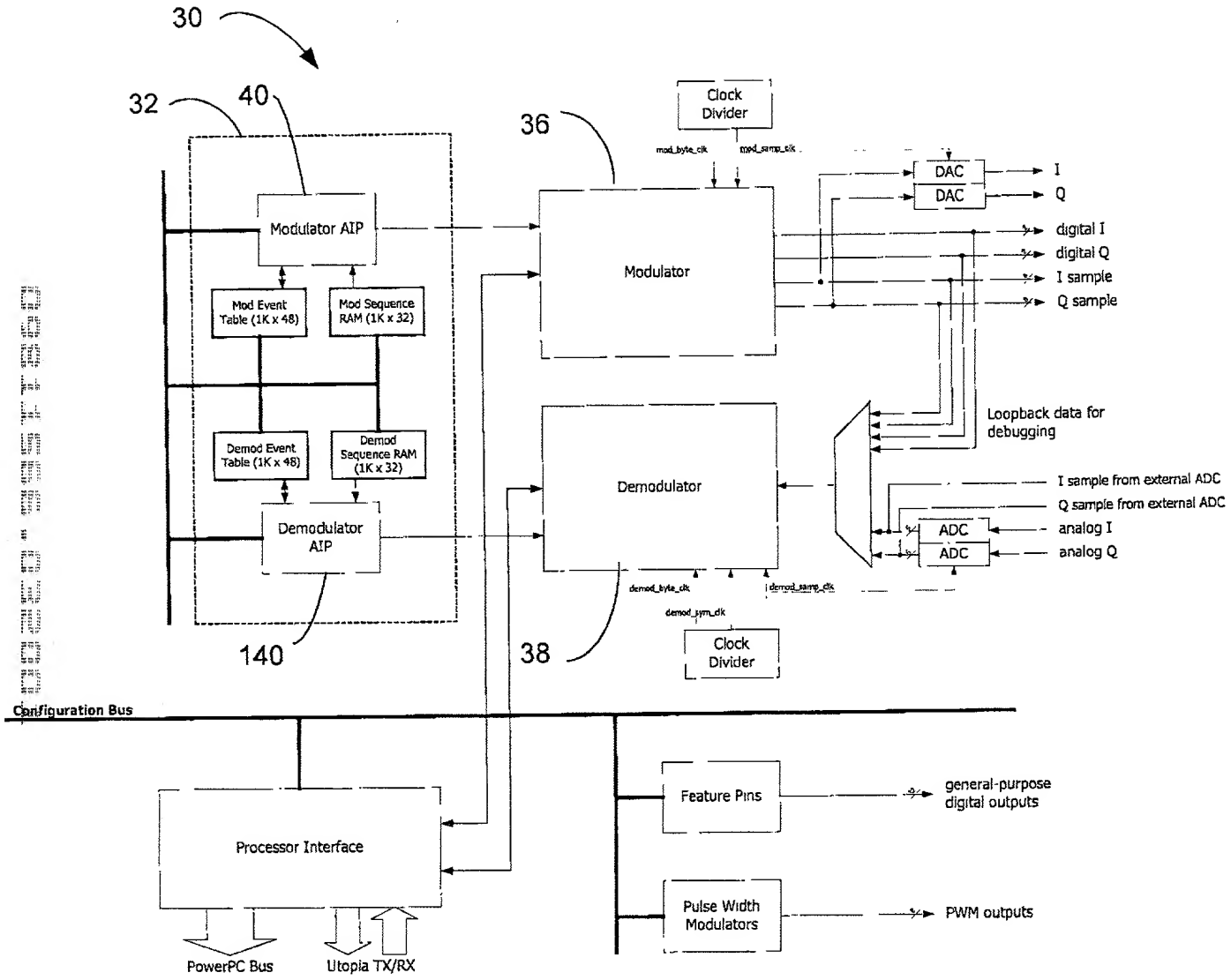

30
32
40
36
Clock Divider
mod_byte_clk
mod_samp_clk
DAC
DAC
I
Q
Modulator AIP
Modulator
digital I
digital Q
I sample
Q sample
Mod Event Table (1K x 48)
Mod Sequence RAM (1K x 32)
Demod Event Table (1K x 48)
Demod Sequence RAM (1K x 32)
Demodulator
Loopback data for debugging
I sample from external ADC
Q sample from external ADC
ADC
ADC
analog I
analog Q
Demodulator AIP
demod_byte_clk
demod_samp_clk
demod_sym_clk
Clock Divider
140
38
Configuration Bus
Processor Interface
Feature Pins
general-purpose digital outputs
Pulse Width Modulators
PWM outputs
PowerPC Bus
Utopia TX/RX

Figure 1

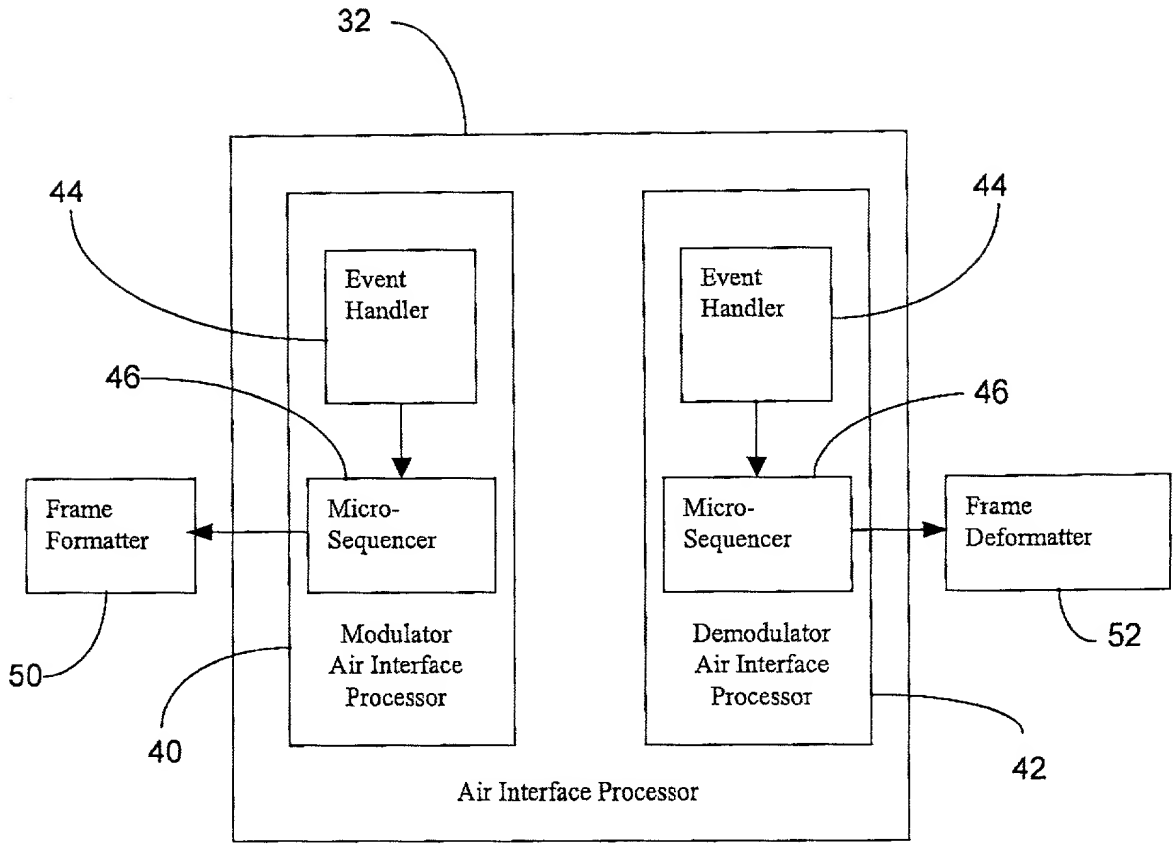
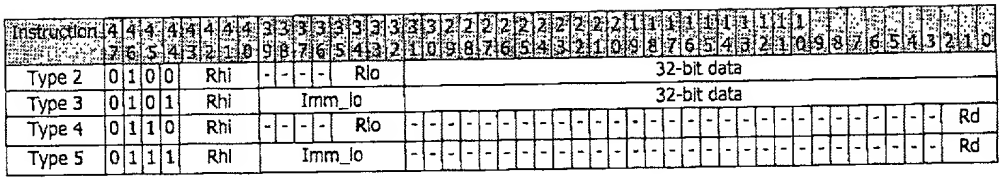

32
44
Event Handler
46
Frame Formatter
Micro-Sequencer
50
Modulator Air Interface Processor
40
44
Event Handler
46
Micro-Sequencer
Frame Deformatter
52
Demodulator Air Interface Processor
42
Air Interface Processor

Figure 2

<table>
<tr><th>Instruction</th><th>47</th><th>46</th><th>45</th><th>44</th><th>43</th><th>42</th><th>41</th><th>40</th><th>39</th><th>38</th><th>37</th><th>36</th><th>35</th><th>34</th><th>33</th><th>32</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>Type 1</td><td>0</td><td>0</td><td colspan="4">ALU opcode</td><td>S</td><td>W</td><td colspan="3">Rd</td><td colspan="4">Rn</td><td colspan="13">operand 2</td><td colspan="4">branch code</td><td colspan="8">pass address</td><td colspan="8">fail address</td></tr>
<tr><td>Type 2</td><td>0</td><td>1</td><td>0</td><td>0</td><td colspan="4">Rhi</td><td colspan="4">-</td><td colspan="4">Rlo</td><td colspan="32">32-bit data</td></tr>
<tr><td>Type 3</td><td>0</td><td>1</td><td>0</td><td>1</td><td colspan="4">Rhi</td><td colspan="8">Imm_lo</td><td colspan="32">32-bit data</td></tr>
<tr><td>Type 4</td><td>0</td><td>1</td><td>1</td><td>0</td><td colspan="4">Rhi</td><td colspan="4">-</td><td colspan="4">Rlo</td><td colspan="29">-</td><td colspan="3">Rd</td></tr>
<tr><td>Type 5</td><td>0</td><td>1</td><td>1</td><td>1</td><td colspan="4">Rhi</td><td colspan="8">Imm_lo</td><td colspan="29">-</td><td colspan="3">Rd</td></tr>
<tr><td>Type 6</td><td>1</td><td>T</td><td>D</td><td colspan="2">Q</td><td>0</td><td colspan="10">Microsequencer address</td><td colspan="32">trigger time</td></tr>
<tr><td>Type 7</td><td>1</td><td colspan="3">-</td><td>0</td><td>1</td><td colspan="2">-</td><td colspan="40">burst info</td></tr>
<tr><td>Type 8</td><td>1</td><td colspan="2">-</td><td>A</td><td>1</td><td>1</td><td colspan="26">-</td><td colspan="16">mask</td></tr>
</table>

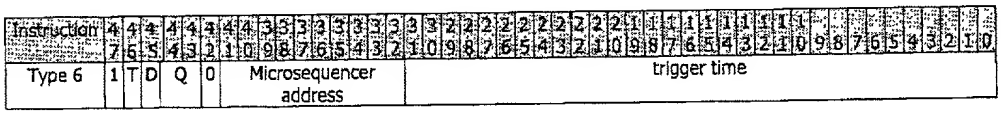
Instruction Type 1: ALU Operations
Instruction Type 2: Write register
Instruction Type 3: Write register immediate
Instruction Type 4: Read register
Instruction Type 5: Read register immediate
Instruction Type 6: Trigger
Instruction Type 7: BURST
Instruction Type 8: WAIT
[A='0' → until any of (R12 and mask) bits are set]
[A='1' → until all of (R12 and mask) bits are set]

Figure 3: Event Handler Instruction Set Summary



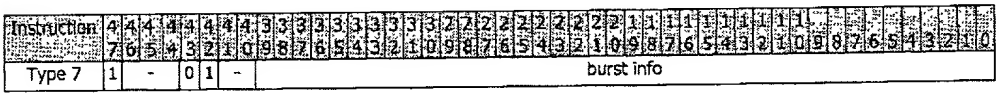
Instruction	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Type 2	0	1	0	0	Rhi								Rlo		32-bit data																																	
Type 3	0	1	0	1	Rhi								Imm_lo		32-bit data																																	
Type 4	0	1	1	0	Rhi								Rlo																																			Rd
Type 5	0	1	1	1	Rhi								Imm_lo																																			Rd

Figure 4: Register Access Instructions



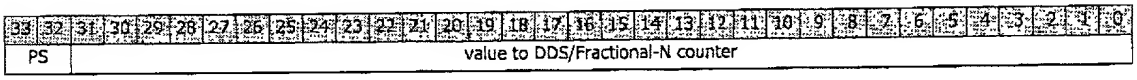
Instruction	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Type 6	1	T	D	Q	0	Microsequencer address																									trigger time																		

Figure 5: Data Scheduling Instructions



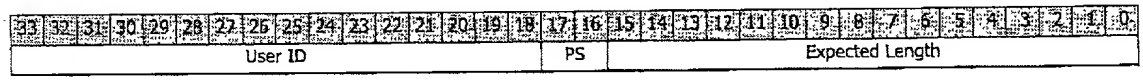
Instruction	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Type 7	1	-			0	1	-	burst info																																										

Figure 6: Burst Descriptor Instruction



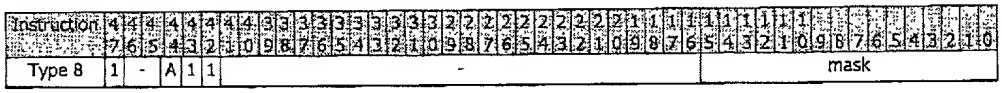
33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PS	value to DDS/Fractional-N counter																																

Figure 7: Modulator Burst Info Field Format



33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
User ID																PS		Expected Length															

Figure 8: Demodulator Burst Info Field Format



Instruction	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Type 8	1	-	A	1	1	-	mask																																										

Figure 9: Processor Wait Instruction

opcode	name	Description
00000	JZ	Jump to Zero
00001	CJS	Conditional Jump to Subroutine
00010	JMAP	Jump Map
00011	CJP	Conditional Jump Pipeline
00100	PUSH	Push/Conditional Load Counter
00101	JSRP	Conditional Jump to Subroutine
00110	CJV	Conditional Jump Vector
00111	JRP	Conditional Jump
01000	RFCT	Repeat Loop Counter Not Equal to Zero
01001	RPCT	Repeat Pipeline Counter Not Equal to Zero
01010	CRTN	Conditional Return
01011	CJPP	Conditional Jump Pipeline and Pop
01100	LDCT	Load Counter and Continue
01101	LOOP	Test End of Loop
01110	CONT	Continue
01111	TWB	Three Way Branch
10000	FORK	Multiway Branch
others		reserved

Figure 10: Microsequencer Instruction Set

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPCODE					EMIT										CCSEL				CP	FFCMD									SB	OC		-	SR

Figure 11: Microsequencer memory format

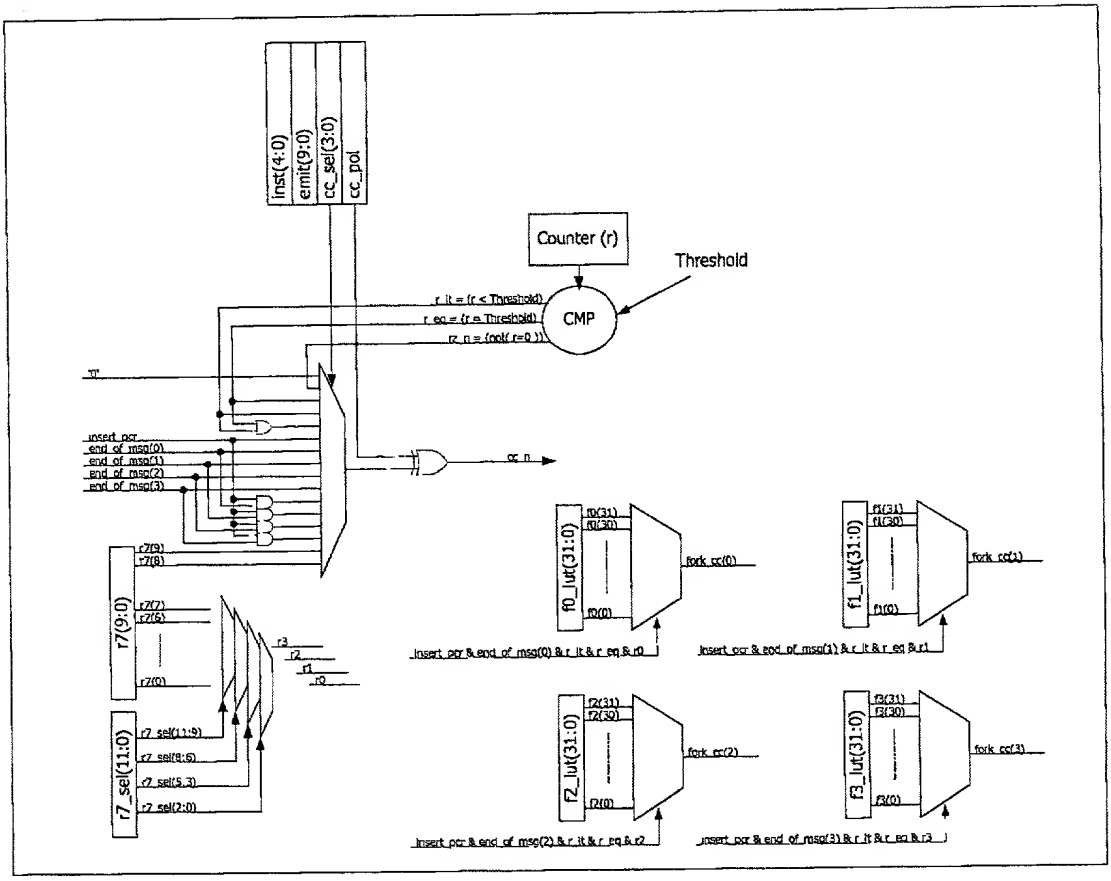


Figure 12: Configuration of condition codes and fork

1	x	x	1	x	Match	
0	0	0	0	0	0	0
0	0	0	0	1	0	
0	0	0	1	0	0	
0	0	0	1	1	0	
0	0	1	0	0	0	0
0	0	1	0	1	0	
0	0	1	1	0	0	
0	0	1	1	1	0	
0	1	0	0	0	0	0
0	1	0	0	1	0	
0	1	0	1	0	0	
0	1	0	1	1	0	
0	1	1	0	0	0	0
0	1	1	0	1	0	
0	1	1	1	0	0	
0	1	1	1	1	0	
1	0	0	0	0	0	C
1	0	0	0	1	0	
1	0	0	1	0	1	
1	0	0	1	1	1	
1	0	1	0	0	0	C
1	0	1	0	1	0	
1	0	1	1	0	1	
1	0	1	1	1	1	
1	1	0	0	0	0	C
1	1	0	0	1	0	
1	1	0	1	0	1	
1	1	0	1	1	1	
1	1	1	0	0	0	C
1	1	1	0	1	0	
1	1	1	1	0	1	
1	1	1	1	1	1	

Figure 13

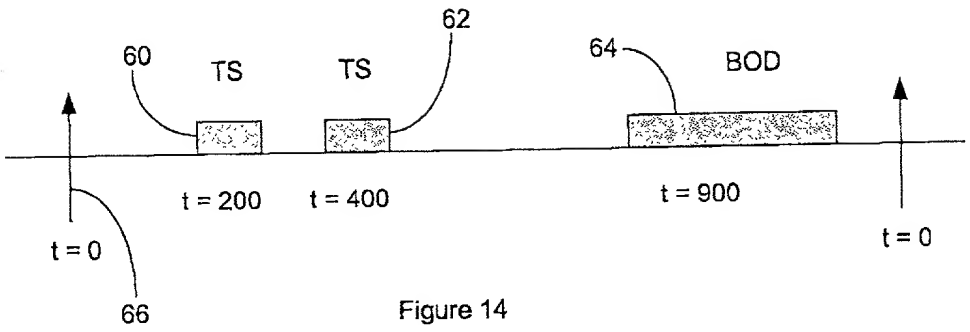


Figure 14

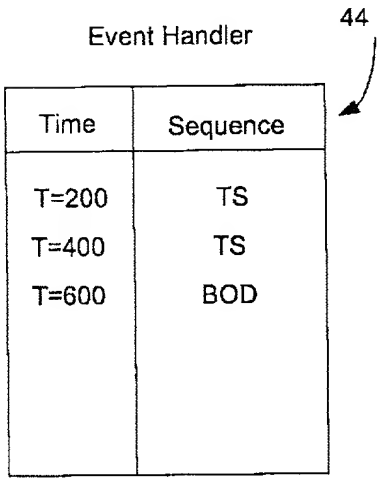


Figure 15

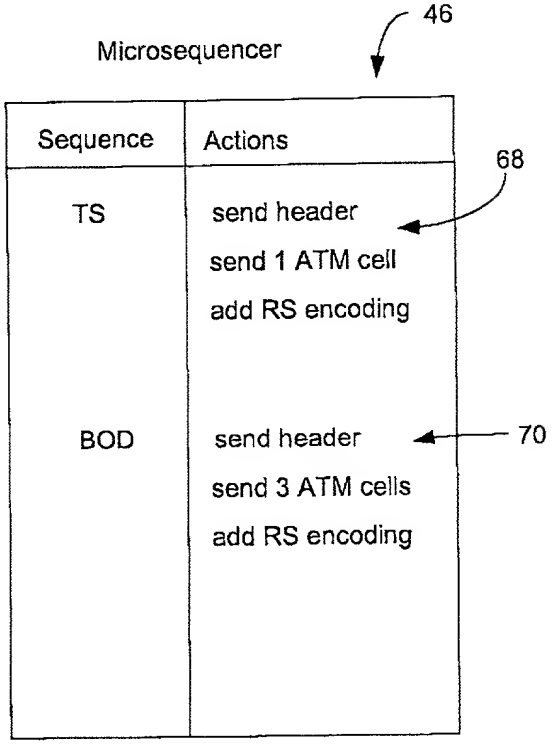


Figure 16

Terminal Modulator Block Diagram

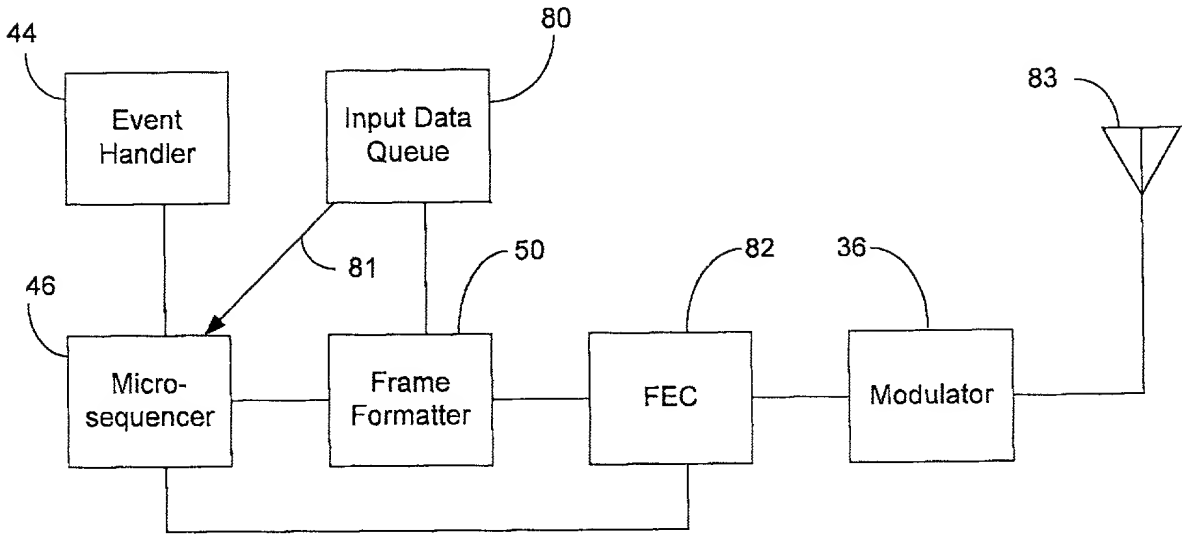


Fig 17

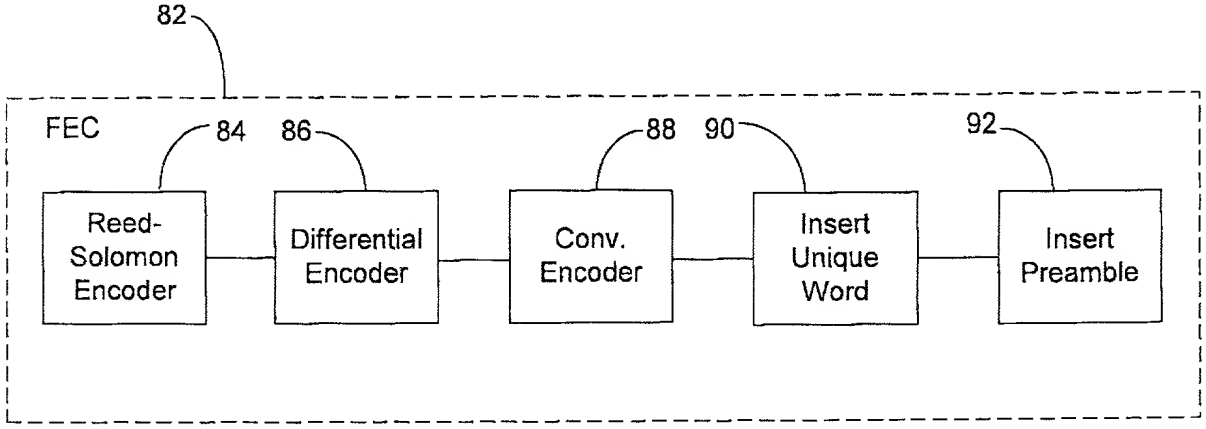


Fig 18

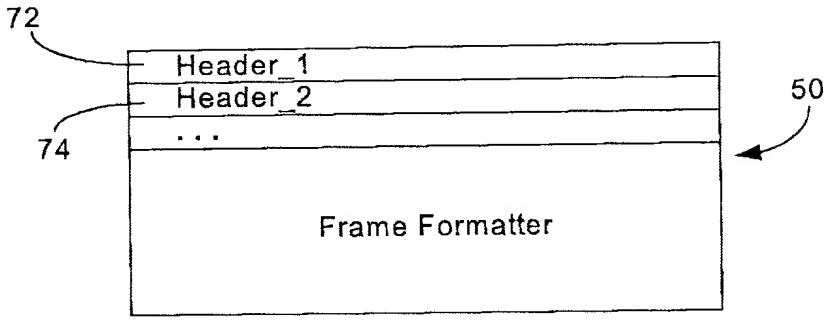


Figure 19

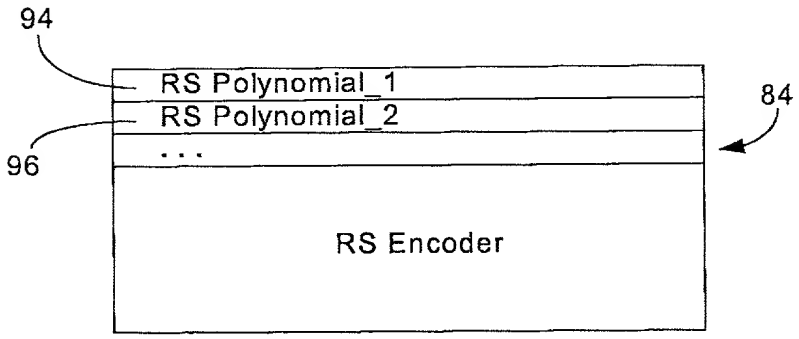


Figure 20

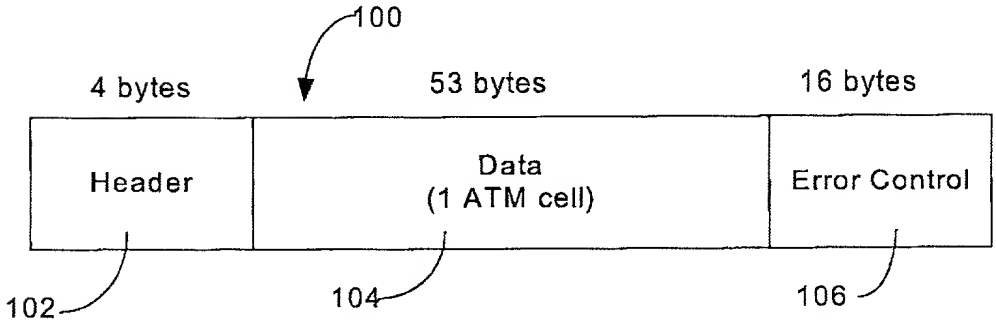


Figure 21

Terminal Demodulator Block Diagram

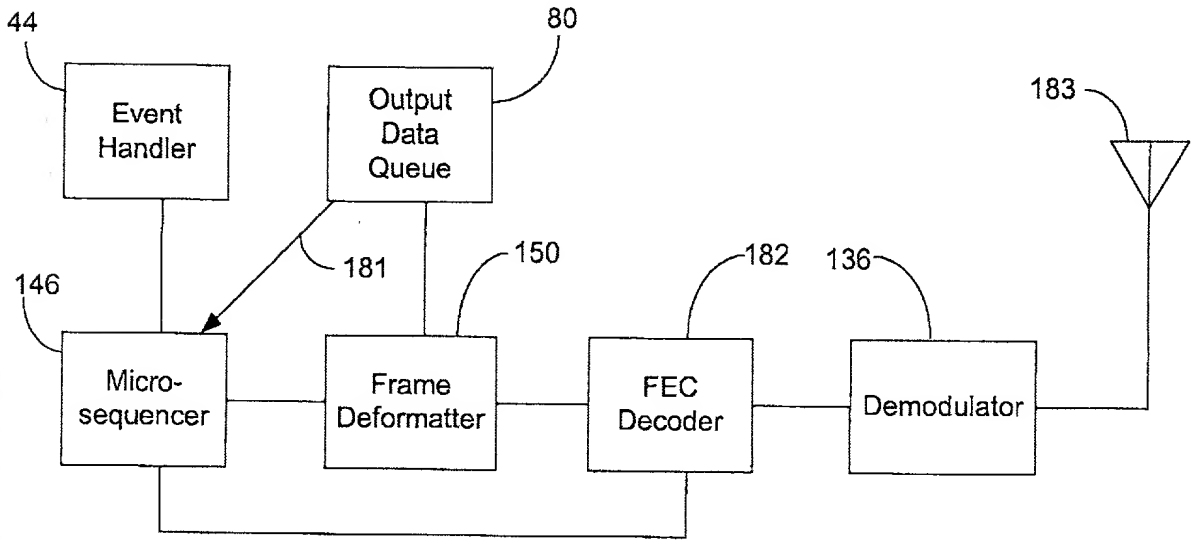


Fig 22

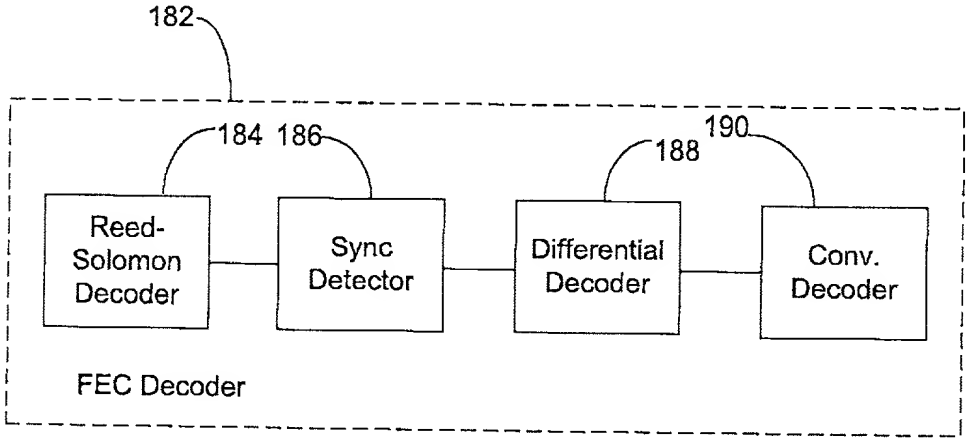


Fig 23